What is claimed is:

[Claim 1] 1. A method for evaluating minority carrier transmission in a semiconductor chip design, comprising the steps of:

forming said semiconductor chip design using shapes;

defining an arc between a first point and a second point in said semiconductor chip design, wherein said arc crosses at least one of said shapes;

defining one or more domains in relation to points on said arc;

quantifying absorption, reflection and transmission characteristics of each domain along said arc; and

evaluating total minority carrier transmission from said first point to said second point across said domains.

[Claim 2] 2. The method of claim 1 wherein each of said domains is delimited by two normal planes.

[Claim 3] 3. The method of claim 2, wherein each of said two normal planes includes a point co-located on said arc and on a perimeter of a shape.

[Claim 4] 4. The method of claim 2, wherein each of said two normal planes includes a bisector of a section of said arc, wherein said section is located between two adjacent points.

[Claim 5] 5. The method of claim 1, further comprising the step of removing shapes that are not in the substrate prior to said step of defining said arc.

[Claim 6] 6. The method of claim 1, further comprising the step of removing shapes within a well tub of a second doping polarity prior to said step of defining said arc.

[Claim 7] 7. The method of claim 1 further comprising the step of calculating electron current collected at said second point.

[Claim 8] 8. The method of claim 1 wherein said first point and said second point lie on a boundary of a circuit.

[Claim 9] 9. The method of claim 1, further comprising the step of relating said arc to a pnpn structure.

[Claim 10] 10. The method of claim 1, wherein said step of evaluating is carried out by calculating a transmission matrix for total minority carrier transmission across said domains.

[Claim 11] 11. The method of claim 10, wherein said transmission matrix is a higher order matrix.

[Claim 12] 12. A method for evaluating minority carrier transmission across an array of unit cells in a semiconductor chip design, comprising the steps of:

a) forming said semiconductor chip design using shapes;

b) evaluating, for each of said unit cells, minority carrier transmission across said unit cell by:

defining an arc between a first point and a second point, wherein said first point and said second point are located on a boundary of said unit cell, and wherein said arc crosses at least one of said shapes;

defining one or more domains in relation to points on said arc;

quantifying absorption, reflection and transmission characteristics of each domain along said arc; and

calculating an individual value for minority carrier transmission from said first point to said second point across said domains for said unit cell;

c) defining a second arc from a point A to a point B across said array of unit cells; and

d) evaluating total minority carrier transmission along said arc by multiplying together individual values of minority transmission for all unit cells in said array of unit cells along said second arc.

[Claim 13] 13. The method of claim 10 wherein each of said domains is delimited by two normal planes.

[Claim 14] 14. The method of claim 11, wherein each of said two normal planes includes one of said points co-located on said arc and on a perimeter of a shape.

[Claim 15] 15. The method of claim 11, wherein each of said two normal planes includes a bisector of a section of said arc, wherein said section is located between two adjacent points.

[Claim 16] 16. The method of claim 10, further comprising the step of removing shapes that are not in the substrate prior to said step of defining said arc.

[Claim 17] 17. The method of claim 10, further comprising the step of removing shapes within a well tub of a second doping polarity prior to said step of defining said arc.

[Claim 18] 18. The method of claim 10, wherein said unit cells are parameterized cells.

[Claim 19] 19. The method of claim 10, wherein said array of unit cells is selected from the group consisting of DRAM arrays, SRAM arrays, decoupling capacitors, off-chip driver (OCD) banks, receiver banks, ESD input networks, ESD power clamps, analog circuitry, gate array logic regions, custom logic, voltage islands, wiring bays, fill shapes, p-cell libraries, and periodic circuit functions.

[Claim 20] 20. The method of claim 10, further comprising the step of relating said arc to a pnpn structure.

[Claim 21] 21. A computer aided design structure for evaluation of latchup and noise, comprising:

a transmission probability generator;

means for relating transmission probability to domains or unit cells, or to domains and unit cells, along an arc; and

means for relating said arc to a pnpn structure.

[Claim 22] 22. The computer aided design structure of Claim 10, further comprising elements selected from the group consisting of a graphical generator; a schematic generator; a technology data file source; a parasitic element identifier; a latchup criteria discriminator, a graph theory generator of parasitic pnpn elements; a current generator of secondary currents initiated by elements that undergo latchup; a primary current and secondary currents summing structure; a tree propagation generator; and a latchup propagation evaluator.

[Claim 23] 23. A computer aided design apparatus, comprising:

a graphics generator;

a schematic generator; and

a graphical unit interface containing a parameterized cell, wherein said parameterized cell is defined by said graphics generator and said schematic generator and contains transmission, absorption, and reflection parameters corresponding to said parameterized cell.